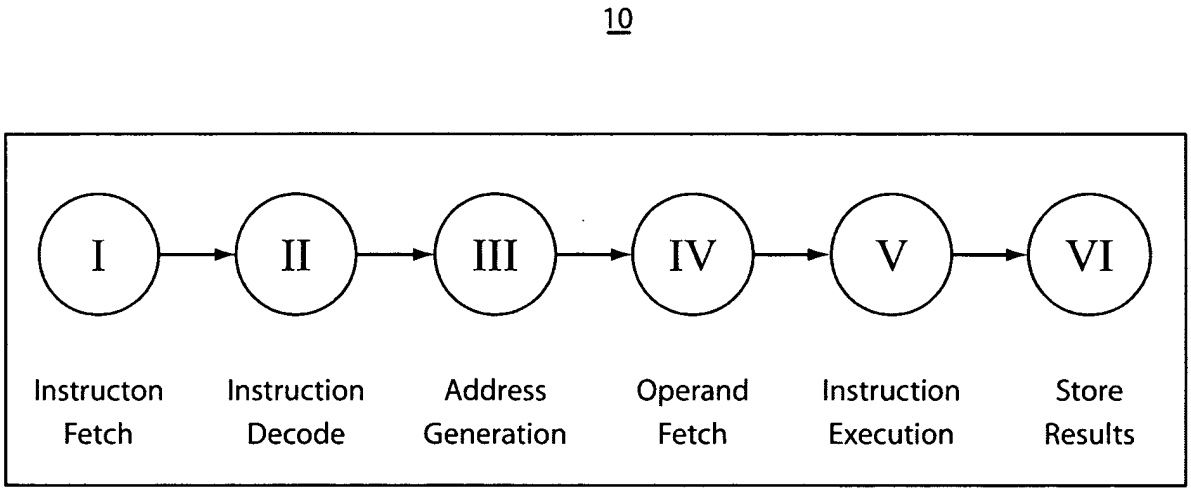

10
I
II
III
IV
V
VI
Instructon Fetch
Instruction Decode
Address Generation
Operand Fetch
Instruction Execution
Store Results

FIG. 1A

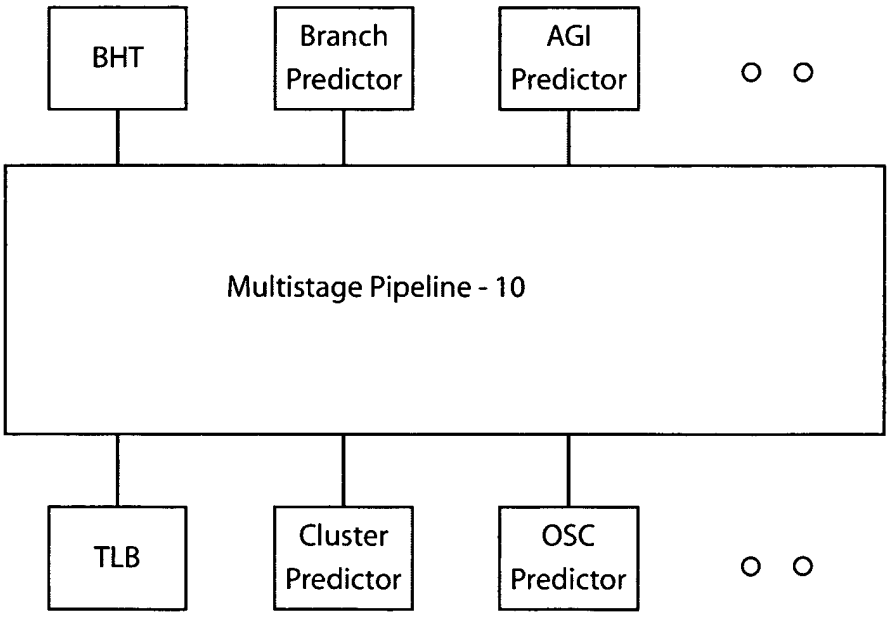

BHT
Branch Predictor
AGI Predictor
Multistage Pipeline - 10
TLB
Cluster Predictor
OSC Predictor

FIG. 1B

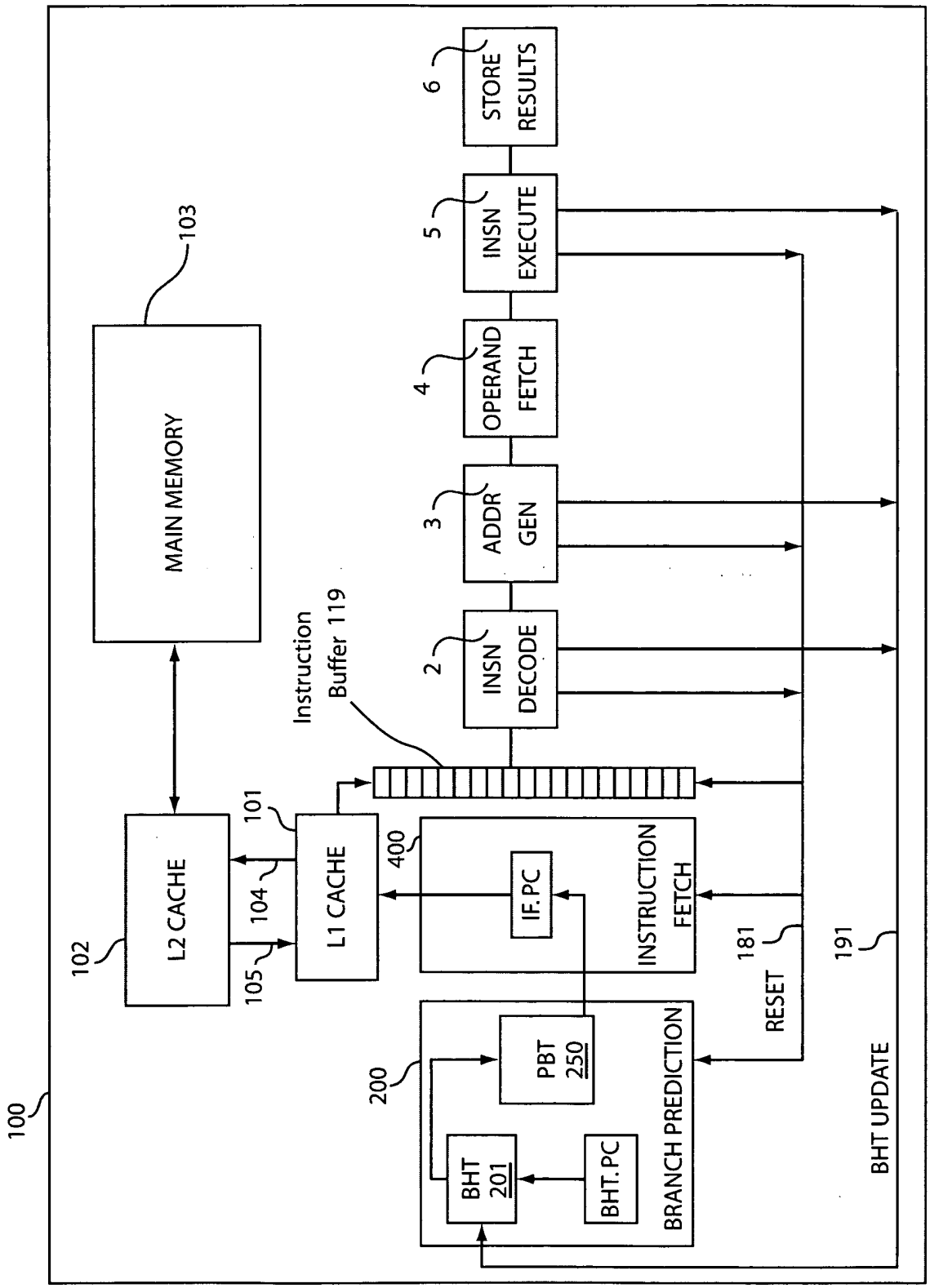

100
MAIN MEMORY
103
L2 CACHE
102
104
105
L1 CACHE
101
Instruction
Buffer 119
INSN
DECODE
2
ADDR
GEN
3
OPERAND
FETCH
4
INSN
EXECUTE
5
STORE
RESULTS
6
400
IF.PC
INSTRUCTION
FETCH
181
RESET
191
BHT UPDATE
200
PBT
250
BHT
201
BHT.PC
BRANCH PREDICTION

FIG. 2

Branch History Table - 201

Branch Instruction Address - 202	Target Address of Branch - 204

FIG.3

Branch Prediction Mechanism - 200

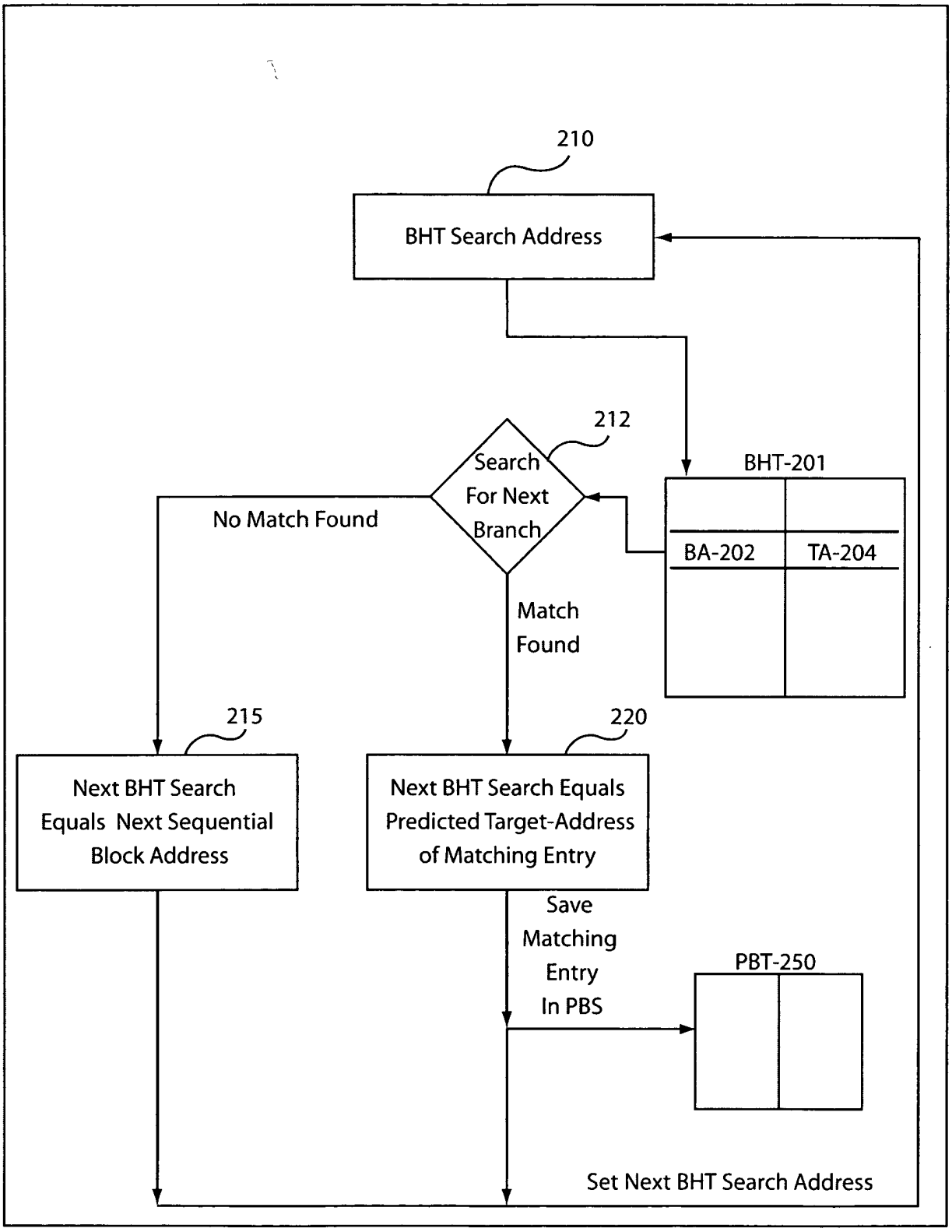


FIG.4

Predicted Branch Table - 250

Instruction Address Of Next Taken Branch (Predicted) - 252	Target Address Of Next Taken Branch (Predicted) - 254

FIG.5

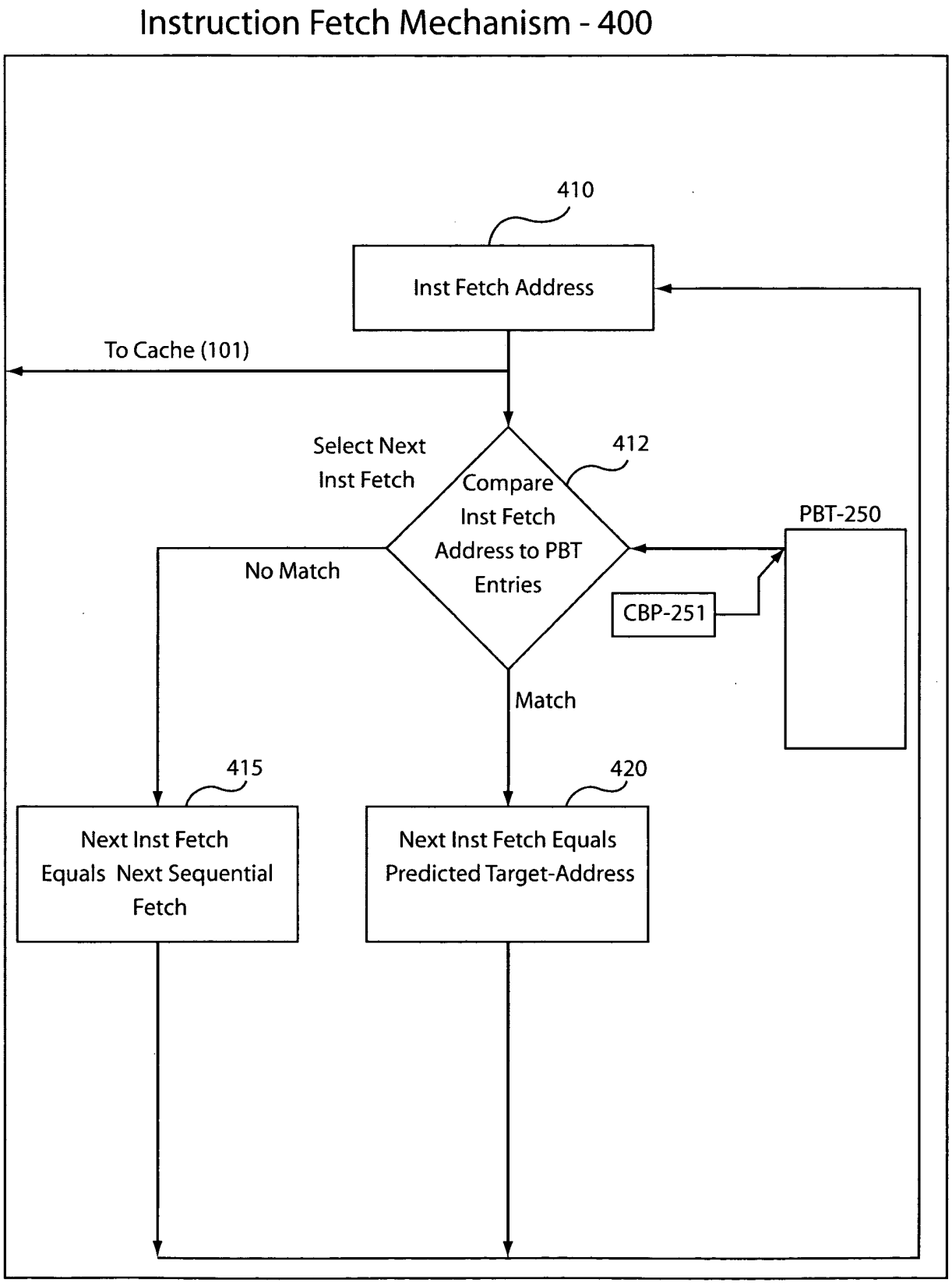

Instruction Fetch Mechanism - 400
410
Inst Fetch Address
To Cache (101)
Select Next Inst Fetch
412
Compare Inst Fetch Address to PBT Entries
PBT-250
No Match
CBP-251
Match
415
420
Next Inst Fetch Equals Next Sequential Fetch
Next Inst Fetch Equals Predicted Target-Address

FIG. 6

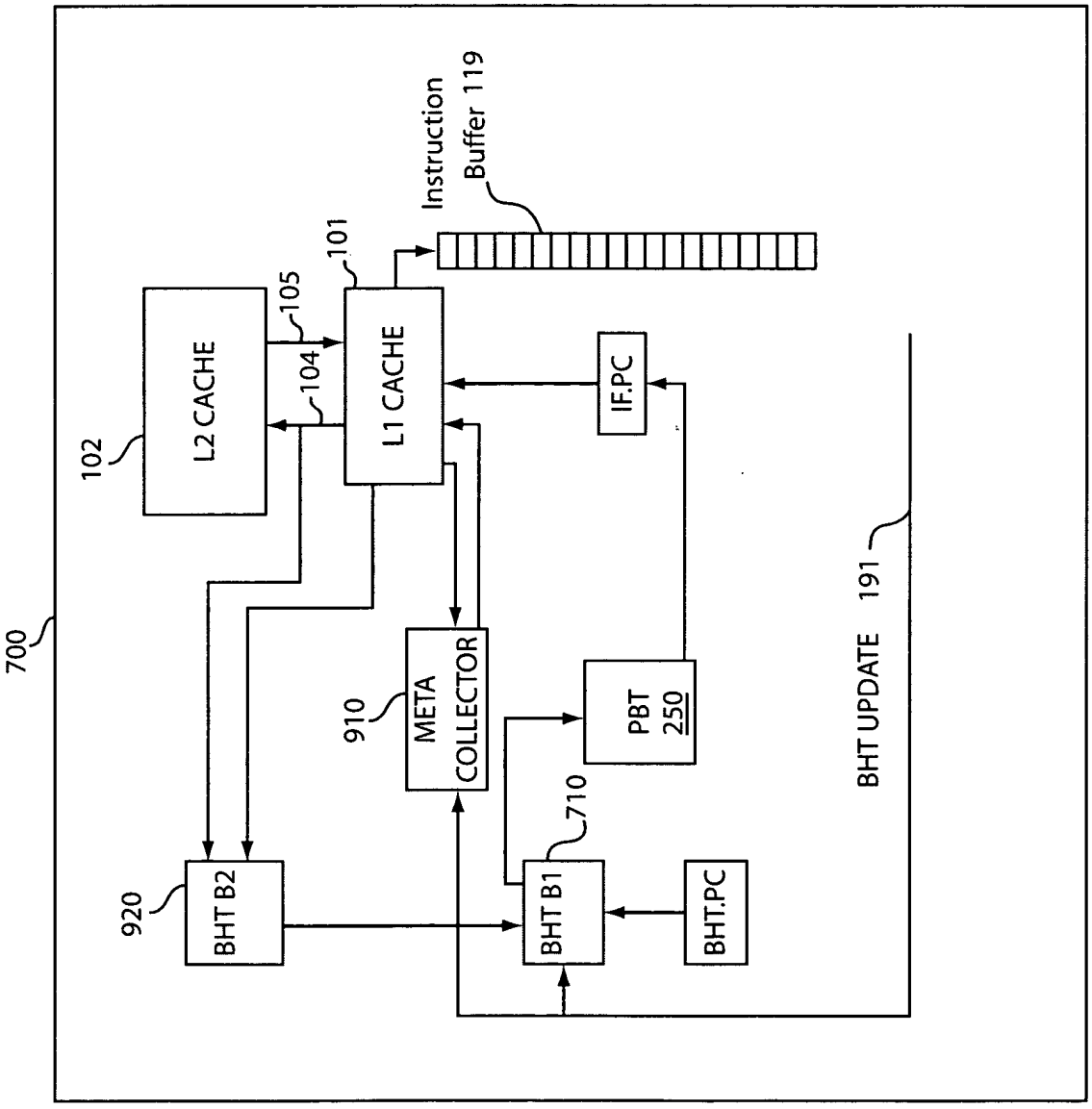
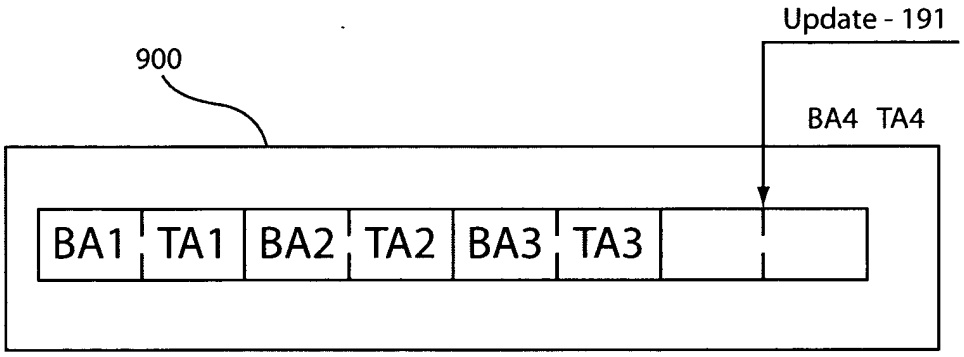

700
Instruction Buffer 119
101
105
104
L2 CACHE
102
L1 CACHE
IF.PC
910
META COLLECTOR
PBT 250
710
BHT UPDATE 191
920
BHT B2
BHT B1
BHT.PC

FIG. 7



BA1, BA2, BA3, and B4 are distinct and in program order

FIG. 8

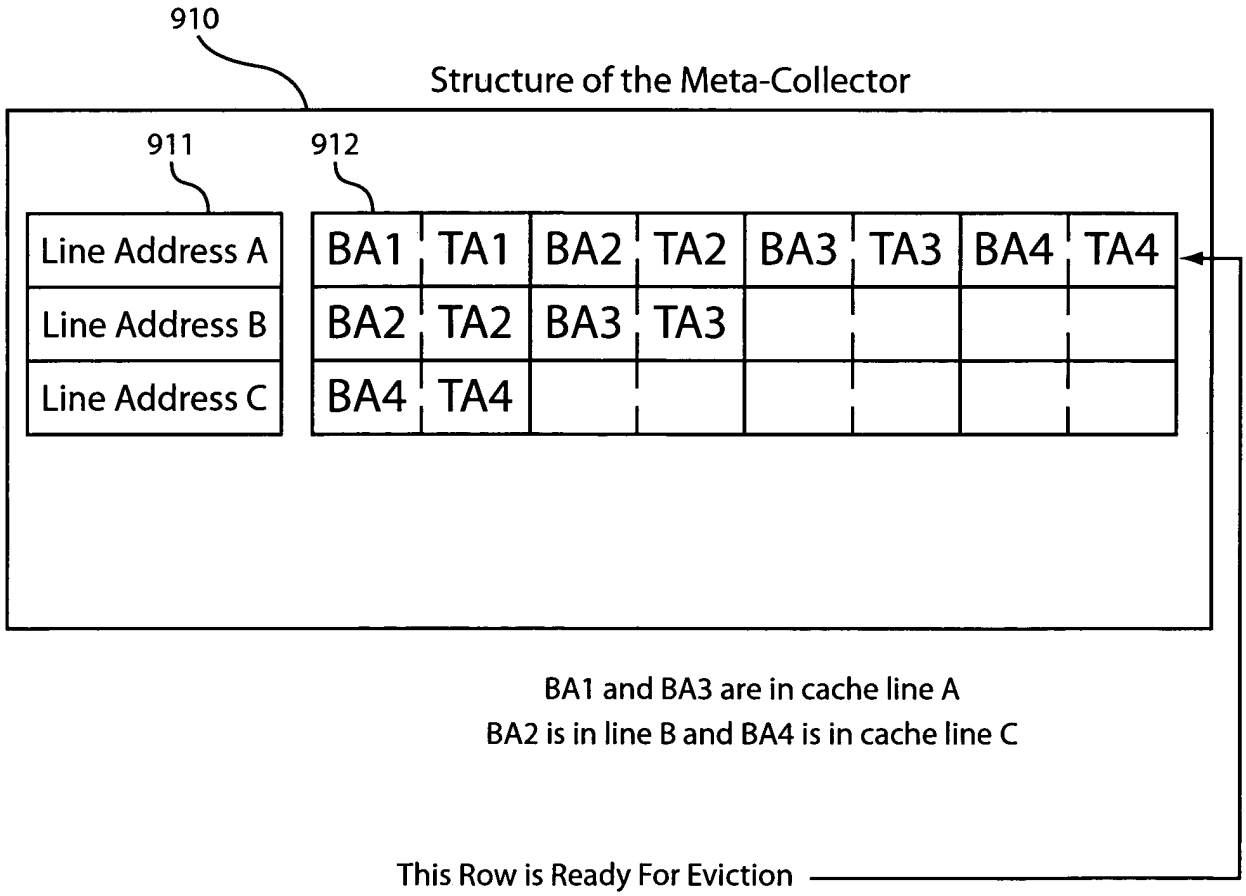

910
Structure of the Meta-Collector
911
912
Line Address A
Line Address B
Line Address C
BA1 TA1 BA2 TA2 BA3 TA3 BA4 TA4
BA2 TA2 BA3 TA3
BA4 TA4
BA1 and BA3 are in cache line A
BA2 is in line B and BA4 is in cache line C
This Row is Ready For Eviction

FIG. 9

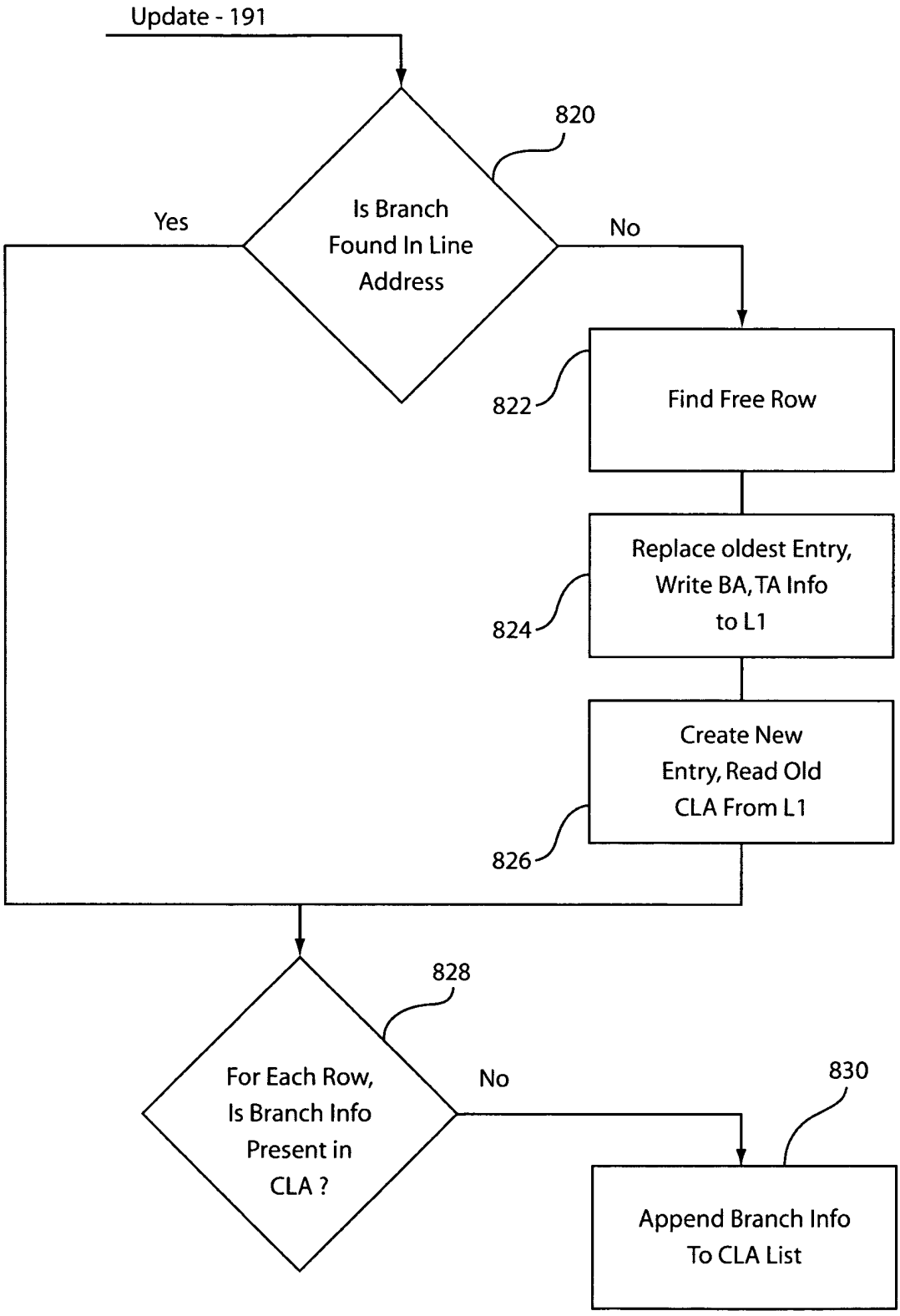

Update - 191
820
Is Branch Found In Line Address
Yes
No
822
Find Free Row
824
Replace oldest Entry, Write BA, TA Info to L1
826
Create New Entry, Read Old CLA From L1
828
For Each Row, Is Branch Info Present in CLA ?
No
830
Append Branch Info To CLA List

FIG. 10

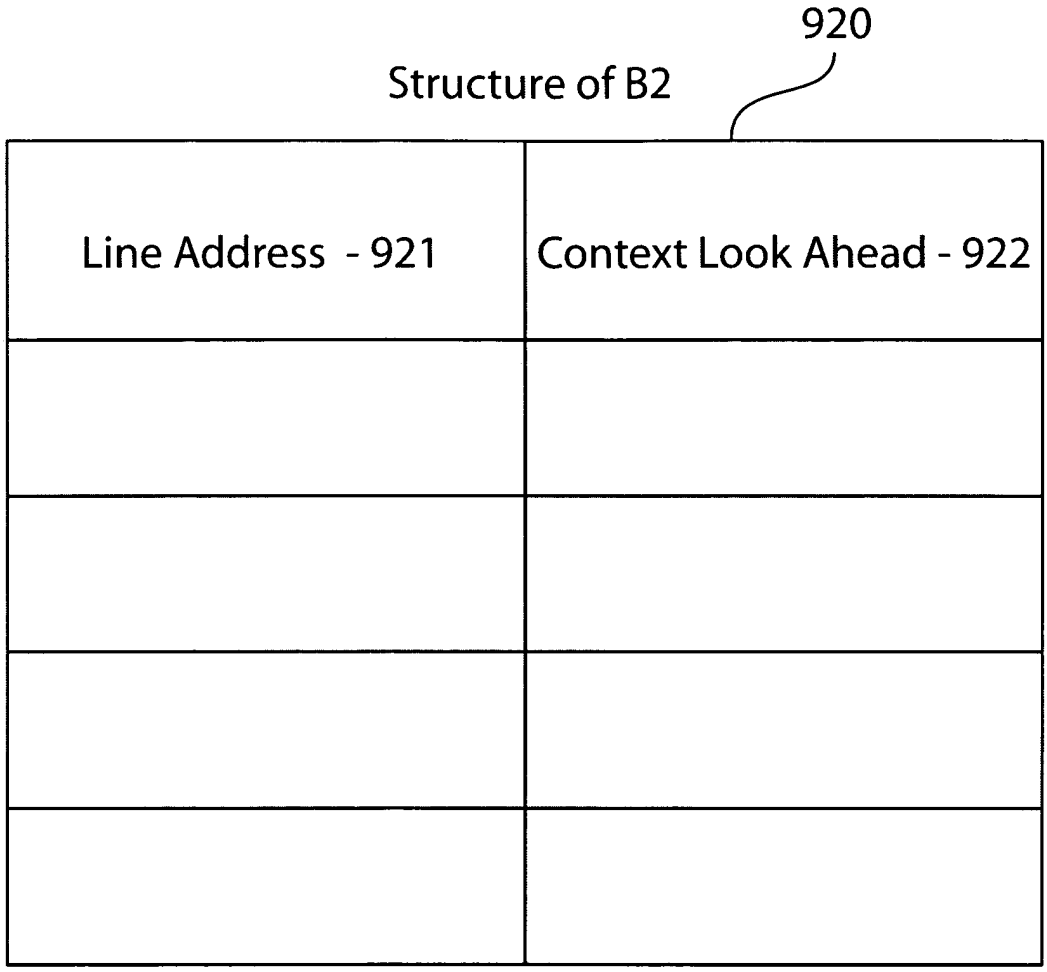


FIG. 11

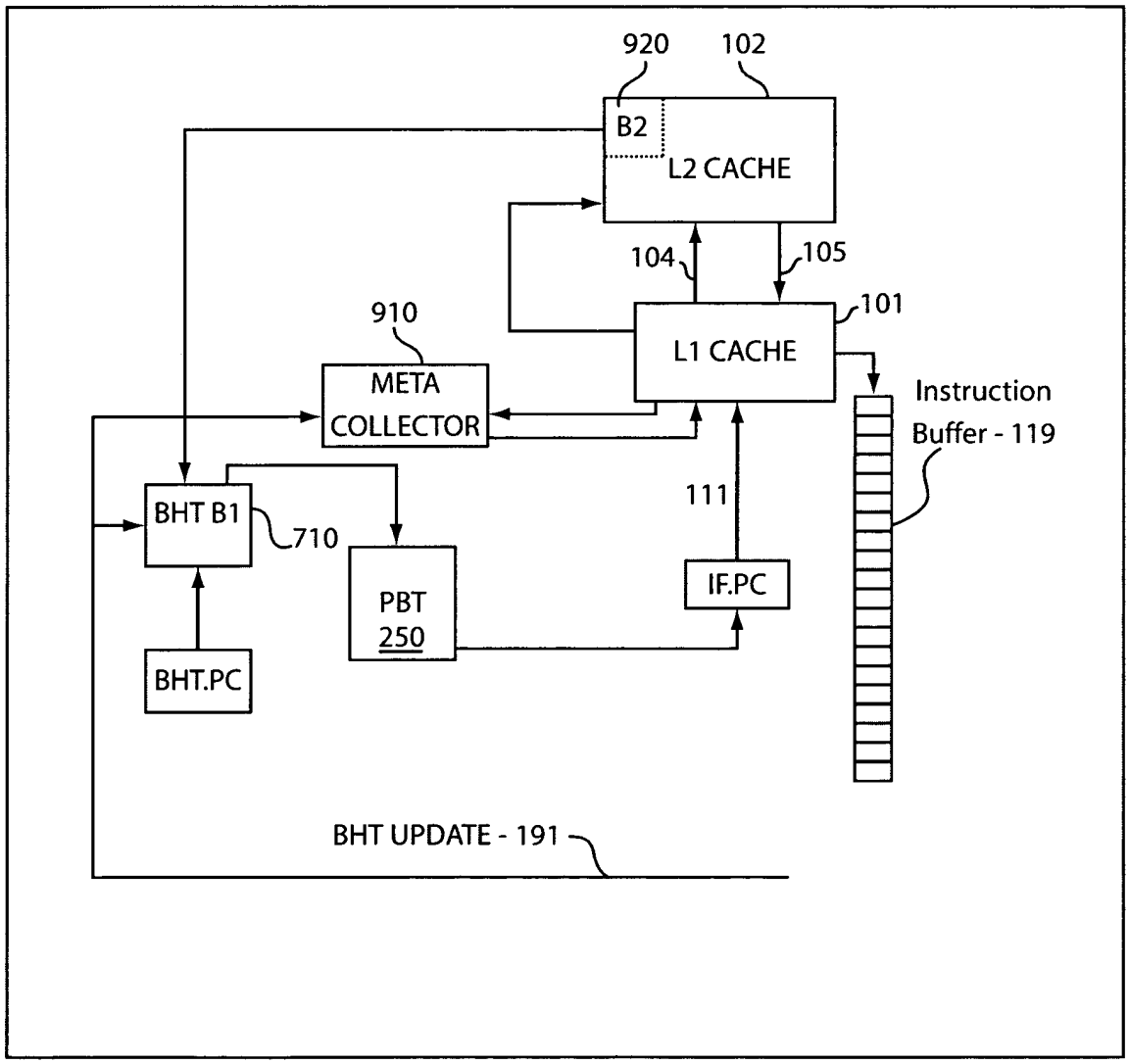

920
102
B2
L2 CACHE
104
105
910
101
L1 CACHE
META
COLLECTOR
Instruction
Buffer - 119
111
BHT B1
710
PBT
250
IF.PC
BHT.PC
BHT UPDATE - 191

FIG. 12

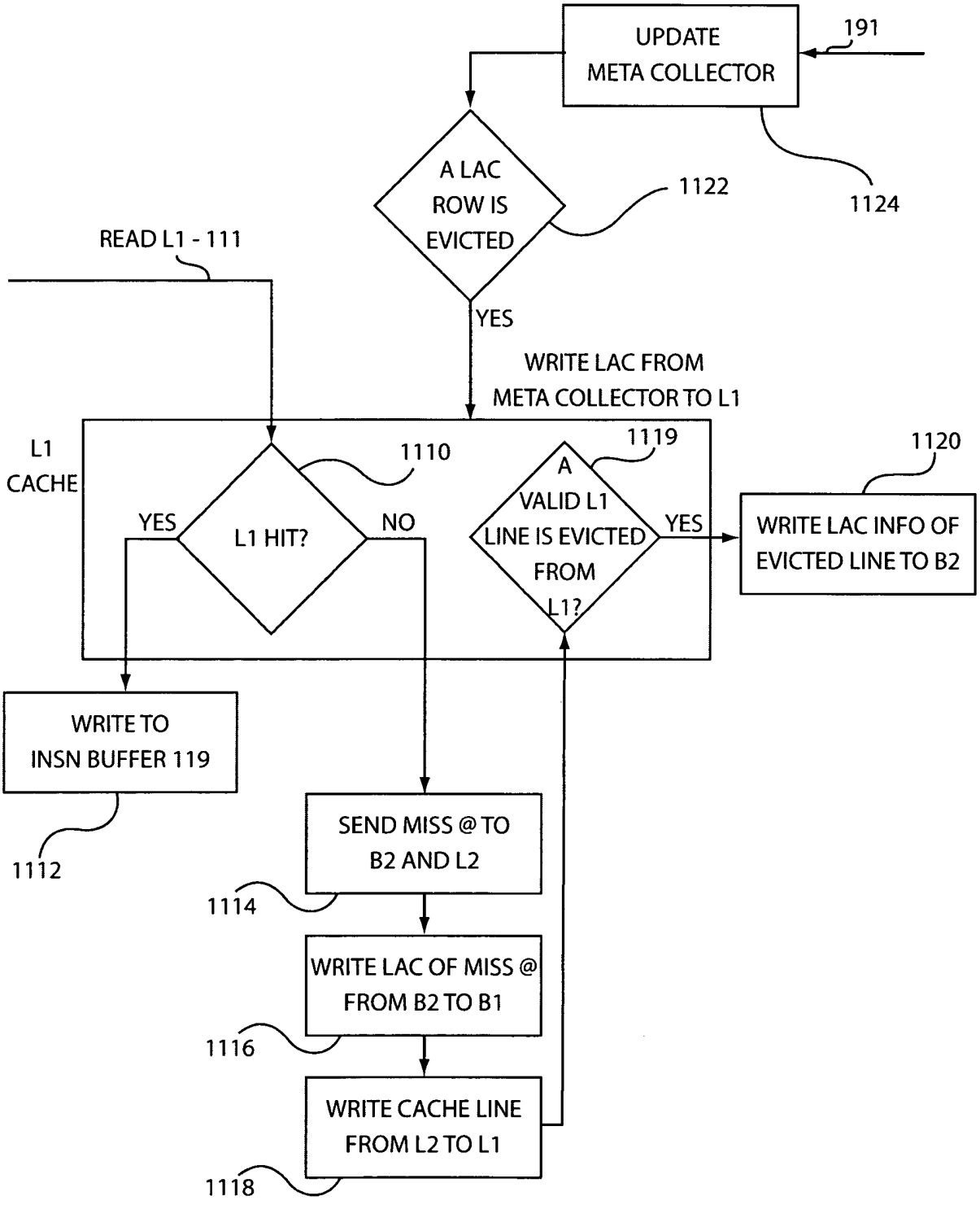

UPDATE
META COLLECTOR
191
A LAC
ROW IS
EVICTED
1122
1124
READ L1 - 111
YES
WRITE LAC FROM
META COLLECTOR TO L1
L1
CACHE
1110
1119
1120
YES
L1 HIT?
NO
A
VALID L1
LINE IS EVICTED
FROM
L1?
YES
WRITE LAC INFO OF
EVICTED LINE TO B2
WRITE TO
INSN BUFFER 119
1112
SEND MISS @ TO
B2 AND L2
1114
WRITE LAC OF MISS @
FROM B2 TO B1
1116
WRITE CACHE LINE
FROM L2 TO L1
1118

FIG. 13

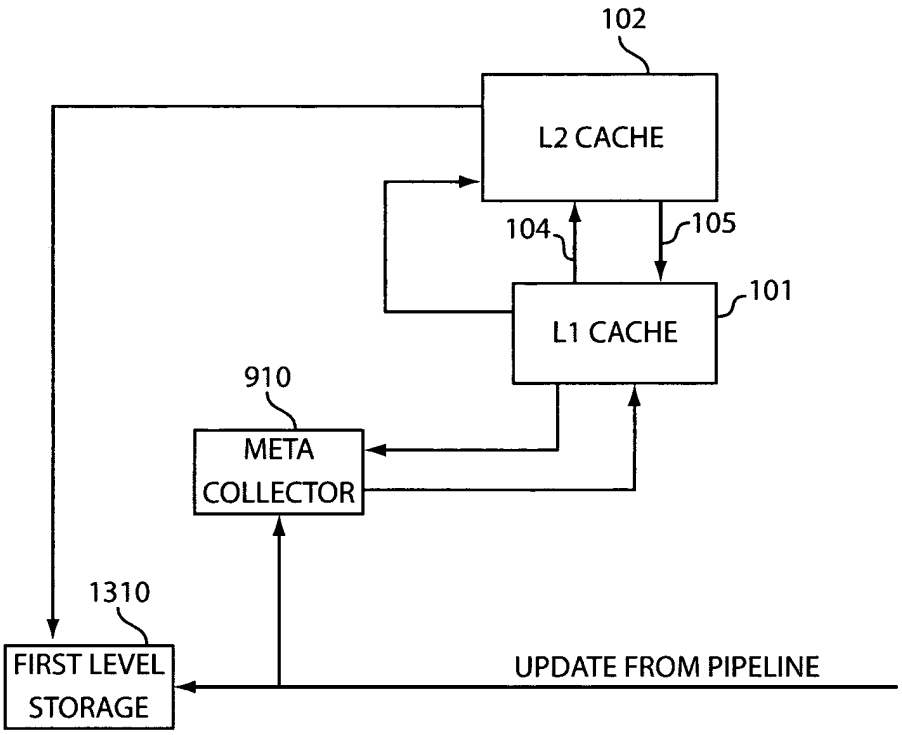

102
L2 CACHE
104
105
101
L1 CACHE
910
META
COLLECTOR
1310
FIRST LEVEL
STORAGE
UPDATE FROM PIPELINE

FIG. 14

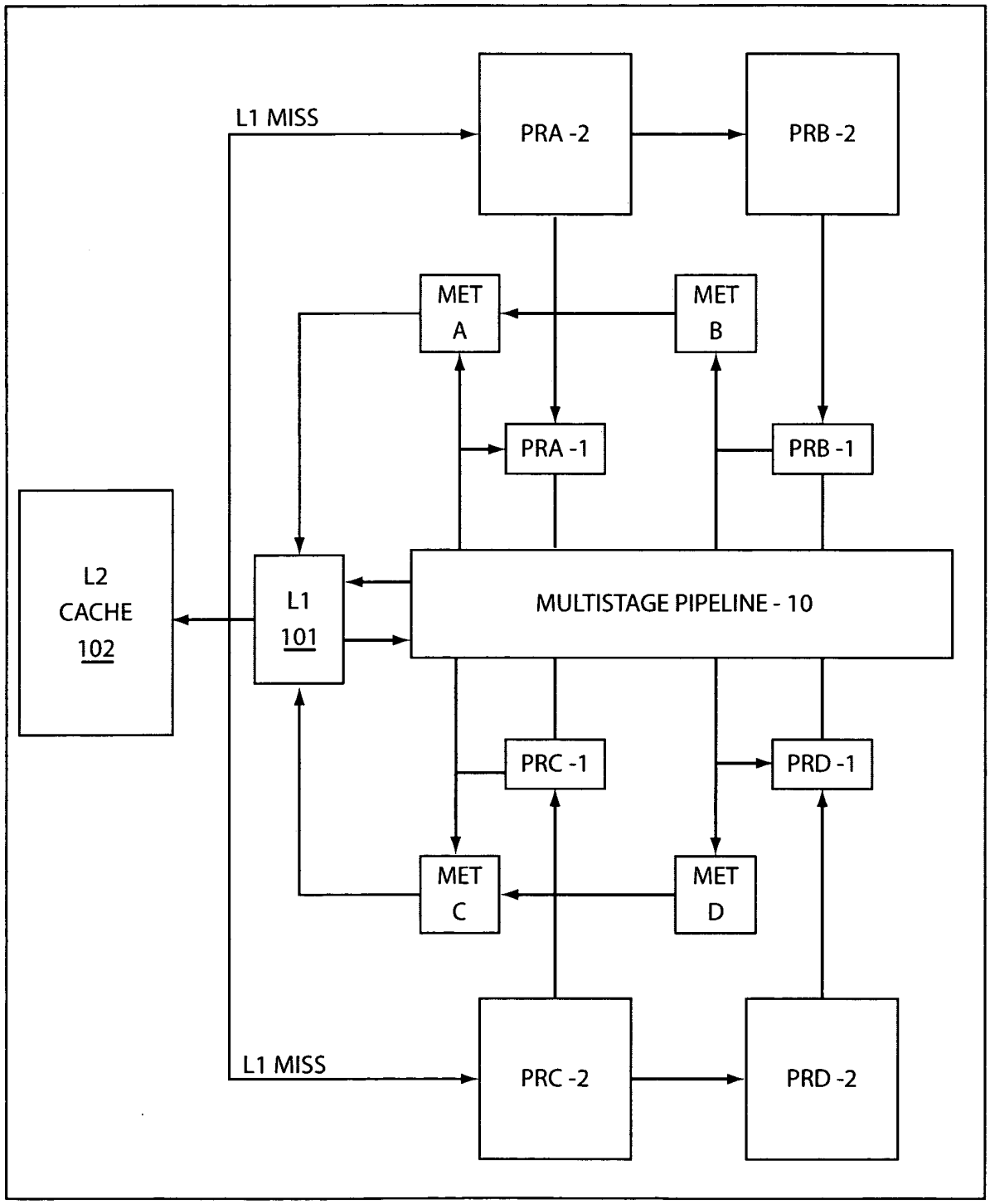

L1 MISS
PRA -2
PRB -2
MET A
MET B
PRA -1
PRB -1
L2 CACHE 102
L1 101
MULTISTAGE PIPELINE - 10
PRC -1
PRD -1
MET C
MET D
L1 MISS
PRC -2
PRD -2

FIG. 15